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(54) Method and apparatus for reordering memory operations in a superscalar or very long instruction word processor

(57) A method and apparatus for reordering memory operations in superscalar or very long instruction word (VLIW) processors is described, incorporating a mechanism that allows for arbitrary distance between reading from memory and using data loaded out-of-order, and that allows for moving load operations earlier in the execution stream. This mechanism tolerates ambiguous memory references. The mechanism executes only one additional instruction for disambiguation purposes, thus producing good performance, and integrates memory disambiguation with speculative execution of instructions. The overhead introduced is only one instruction, and the load operation can be arbitrarily moved earlier in the instruction stream. The mechanism can cope with conflicts that occur as a result of an unexpected combination of store/load instructions, can be used in a coherent multiprocessor context, and combines speculative execution with reordering of memory operations in a way which requires simple hardware support.

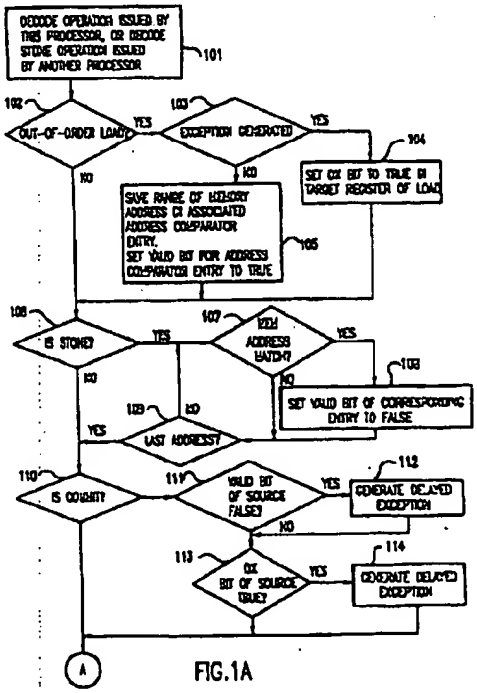

FIG.1A

EP 0 742 512 A2

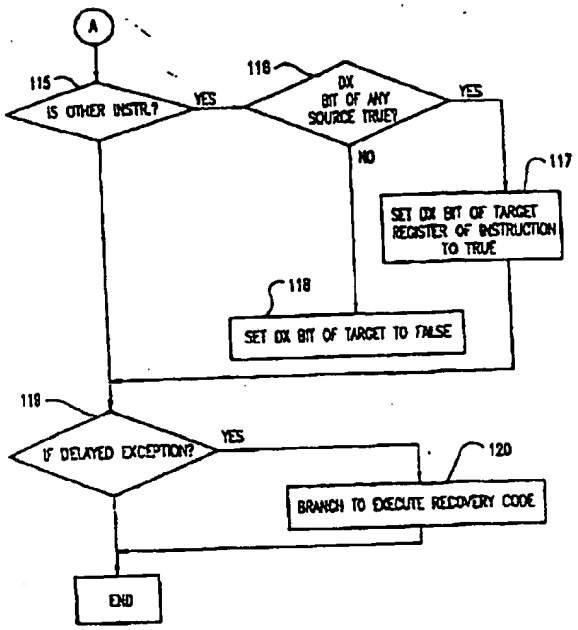

FIG.1B